IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	SETHURAMAN
Application No.	:	10/530,495
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For	:	DATA PROCESSING APPARATUS ADDRESS RANGE DEPENDENT PARALLELIZATION OF INSTRUCTIONS

APPEAL BRIEF

On Appeal from Group Art Unit 2183

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By: Michael Ure
Attorney for Applicant
Registration No. 33,089

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Michael Ure
(Name)

(Signature and Date)

page 2, lines 18-26 of the specification, the instruction execution unit may treat information from the instruction memory as relatively longer instruction words, containing relatively more instructions, when these words come from a range of addresses that refer to instructions from the inner loop of a program; and the instruction execution may treat the information as relatively shorter instruction words, containing relatively fewer instructions, when these words come from another range of addresses. Thus, high parallelism can be realized in the inner loop and high storage efficiency can be realized outside the inner loop, without need for explicit instructions to change the instruction word length when passing into or out of the inner loop. The greater the number of instructions in an instruction word, the greater the likelihood of having to include "no-operation" instructions, reducing storage efficiency.

The following analysis of independent claim 1 is presented for convenience (referring, at the behest of the Examiner, to only a single exemplary embodiment, namely that of Figs. 1-3):

Element	Figure(s)	Paragraph(s) and/or page(s)
1. A data processing apparatus, the apparatus comprising:		
an instruction address generation circuit for outputting an instruction address;	Fig. 1	Page 3, line 31 to page 4, line 11
an instruction memory system arranged to output an instruction word addressed by the instruction address;	Fig. 1; Fig. 2, 12.	Page 3, line 31 to page 4, line 11; page 6, line 27 to page 9, line 2.
an instruction execution unit, arranged to process a	Fig. 1, 14.	Page 3, line 31 to page 4, line 11; page 6, line 27 to

plurality of instructions from the instruction word in parallel;		page 9, line 2.
a detection unit, arranged to detect in which of a plurality of ranges the instruction address lies,	Fig. 1, 16; Fig. 3.	Page 3, line 31 to page 4, line 11; page 9.
the detection unit being coupled to the instruction execution unit and/or the memory system, to control a way in which the instruction execution unit parallelizes processing of the instructions from the instruction word, dependent on a detected range..	Fig. 1, Fig. 2.	Page 4, line 28 to page 5, line 5; page 6, line 27 to page 9.

The following analysis of independent claim 15 is presented for convenience (referring again, at the behest of the Examiner, to only a single exemplary embodiment, namely that of Figs. 1-3):

Element	Figure(s)	Paragraph(s) and/or page(s)
15. A method of executing a program with data processing apparatus, the method comprising:		
using an instruction address to fetch an instruction word;	Fig. 1	Page 3, line 31 to page 4, line 11
executing instructions from the fetched instruction word;	Fig. 1, 14.	Page 3, line 31 to page 4, line 11; page 6, line 27 to page 9.
detecting in which of a plurality of ranges the instruction address lies,	Fig. 1, 16; Fig. 3.	Page 3, line 31 to page 4, line 11; page 9.
controlling a way in which the instruction execution is parallelized dependent on a detected range.	Fig. 1	Page 4, line 28 to page 5, line 5; page 6, line 27 to page 9.